

REMARKS

In the Office Action dated March 31, 2004, the Examiner objected to claim 12, rejected claims 1-3, 5, 12, and 14 under 35 USC 103(a) as unpatentable over Hasegawa (U.S. Patent Publication 2003/0038343) in view of Ishikawa (U.S. Patent 6,583,032), rejected claims 6-8 and 13 under 35 USC 103 as unpatentable over Hasegawa and Ishikawa and further in view of Walker (U.S. Patent No. 6,275,277), rejected claims 10 and 15 under 35 USC 103 as unpatentable over Ishikawa and Ueta (U.S. Patent No. 6,590,919, and rejected claims 11 and 16 under 35 USC 103 over Ishikawa in view of Hahn (U.S. Patent No. 6,131,880). Claims 1-3, 5-8, and 10-16 remain at issue.

The Objected Claims

The undersigned has reviewed claim 12 as amended in the previous response dated February 4, 2004. The typographical errors noted by the Examiner were not identified in the copy of the response in the Applicant's file. The Applicants therefore request that the Examiner double-check these errors. If necessary, the Examiner is encouraged to call the undersigned to discuss any discrepancies.

The Art Rejections

The Applicants disagree with the Examiner's rejection that claims 1-3, 5, 12, and 14 are obvious in view of Hasegawa and Ishikawa

Hasegawa is directed to a Wafer Level Chip Scale Package (WCSP), sometimes referred to as a "flip-chip", where a semiconductor die itself is used as the chip package. After fabrication, the wafer is cut, along the scribe lines, to singulate the individual dice on the wafer. The individual die are then flipped and mounted active-surface down onto a substrate, such as a printed circuit board. Contacts formed on the active surface of the die are soldered to matching solder pads on the board, electro-mechanically coupling the die to the board. The protective resin on the back surface of the die is thus exposed when the die is mounted onto the printed circuit board.

After a WCSP is mounted to a printed circuit board, a visual recognition device is used to inspect the position and height of the chip. With WCSP packages, however, the vision recognition is difficult because the intensity of reflected light of the chip and the printed circuit

board (i.e., contrast) is low. See paragraph [0010] of Hasegawa. To address this problem, Hasegawa proposes the formation of a step-like section formed around the periphery of the back surface of the WCSP. See for example Figure 2 and paragraph [0045].

Figures 12(A) through 12(E) and paragraphs [0101] through [0110] describe the process of forming the step-like section. Figure 12(A) shows the wafer after fabrication. Figure 12B shows the wafer placed over a dicing sheet (1207). The wafer is than back-grinded to form a mirror like surface on the back of the wafer. See paragraphs [0106 and 0107] and Figure 12C. In Figure 12D, an infrared camera 1211 is used to locate the scribe lines on active surface of the wafer. Two wafer scribing operations are then performed on the wafer. Wide, shallow cuts are first made along the scribe lines on the wafer followed by a narrow, deep cut through the wafer. See paragraphs [0108 and 0109]. The result of the two scribing operation result in the step like section illustrated for example in Figure 2. With both scribing operations, the location of the scribe lines are determined by the infrared camera detecting the their location through the thickness of the wafer.

Hasegawa therefore does not teach or suggest:

- i. the application of an opaque material onto the wafer; and
- ii. since there is no opaque material formed on the wafer, Hasegawa fails to teach or suggest the imaging of the wafer through an opaque material.

Ishikawa teaches a method of scribing wafers that involves, as illustrated in Figure 1, the steps of: (i) back-grinding the wafer; (ii) polishing the back surface of the wafer; (iii) forming grooves to a "predetermined depth" on the back surface of the wafer along the saw streets (see Col. 3, lines 10-19); and (iv) singulating the individual die from the wafer using a roller to apply pressure to the wafer. The pressure causes the wafer to break along the grooves in the saw streets (see Col. 4, lines 22-35).

Ishikawa further teaches the use of an infrared irradiating device to locate the saw streets on the wafer. The locations are then provided to a diamond cutter which is used to cut the grooves to the predetermined depth along the saw streets on the wafer. See Col. 3, lines 41-59.

Ishikawa therefore does not anticipate claim 1 in several regards:

i. Ishigawa fails to teach or suggest the application of an opaque material onto the wafer;

ii. Since there is no opaque material formed on the wafer, Ishigawa fails to teach or suggest the imaging of the wafer through an opaque material; and

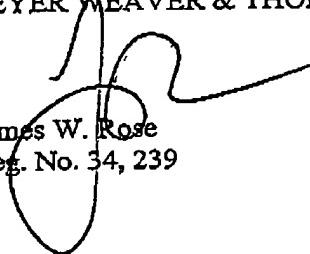
iii. Ishigawa teaches the formation of "grooves" having a "predetermined depth". The grooves cause the wafer to break along the saw streets when pressure is applied to the wafer. Ishigawa therefore actually teaches away from the present invention as claimed which calls for the dicing of the wafer to singulate the individual die on the wafer.

A review of the two references indicates that the Examiner has failed to demonstrate a *prima facia* case of obviousness for a number of reasons. Since both reference fail to teach or suggest the application of an opaque material onto the wafer or the imaging of the wafer to through the opaque material to locate the scribe lines, the rejection is improper. The Applicants therefore submit that claim 1 is allowable. Although patentable in their own right, claims 2, 3 and 5-8 and 10-11 are allowable based on their dependency on claim 1. Similarly, claims 12-16 are allowable for essentially the same reasons as provided above with regard to claim 1.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

James W. Rose
Reg. No. 34, 239



P.O. Box 778
Berkeley, CA 94704-0778
(650) 961-8300